Gumstix DuoVero® Series

System Reference Manual—Version 0.4
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This document describes the Gumstix DuoVero series of computer on modules. Please note that this series is not compatible with the Gumstix Overo COM series.

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This System Reference Manual is a general reference for the Gumstix DuoVero series of Computer-on-Modules (COMs) intended to support:

- **hardware engineers** needing design support for expansion boards, and
- **programmers** writing software that takes advantage of signal multiplexing.

For users just getting started with the Gumstix DuoVero boards, we recommend instead the Getting Started guide http://gumstix.org/get-started/getting-started-guide.html.

This document pertains to all COMs of the Gumstix DuoVero series. For a list of the features available on the different DuoVero COMs, refer to the product information found at www.gumstix.com.

The schematic and layout for expansion boards compatible with DuoVero COMs are freely available online under a Creative Commons license here: http://pubs.gumstix.com/boards/.

Software information can be found online (http://www.gumstix.org/software-development.html).

Note: The products of the Gumstix DuoVero series are NOT compatible with the products of the Gumstix Overo Series.

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1 Product Overview

The Gumstix DuoVero COM delivers ARM Cortex-A9 computing power, up to 1GB of RAM, a microSD card slot and, optionally, wireless communications in this very small and robust form factor.

Based on a common mechanical footprint and a pair of robust 70-pin connectors, any model of DuoVero COM can be mounted on any DuoVero-series expansion board or to a compatible custom-designed expansion boards. The selection of features in openly-available designs includes HDMI, MIPI-compliant camera and display interfaces, Ethernet, USB Host, USB OTG, USB console, stereo audio, a power input jack and breakouts for A/D, GPIO, SPI, PWM, I2C, and 1-wire.

Figure 1 shows the main components of a DuoVero COM which includes a Texas Instruments OMAP™ applications processor (ARM® Cortex™-A9 core), package-on-package (PoP) stack memory, a TWL6030 power management module, a TWL6040 audio codec, interface ICs, and an optional Wi-Fi™ and Bluetooth™ module.

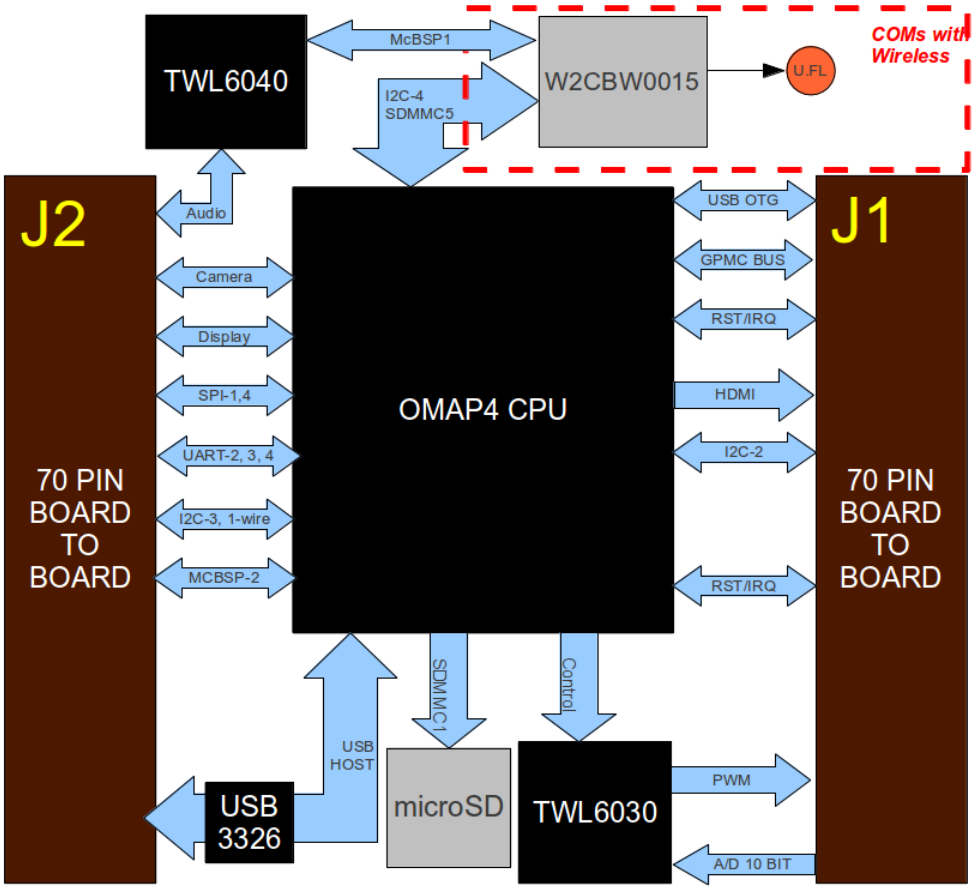

Figure 1: Gumstix DuoVero COM Functional Block Diagram

140 signals from the OMAP4 processor and supporting ICs are broken out via two 70-pin board-to-board connectors called *J1* and *J2*. Section 2 explains these internal interfaces.

Section 3 documents the externally available signals broken out from the Gumstix DuoVero COM. Unless otherwise noted, signals are internally connected to the processor and all general-purpose input-output (GPIO), external memory, reset and interrupt signals are 1.8V logic. Signal names are taken from main functional name from the processor (MUX mode 0) then the standard usage on the COM or as allocated for the most common external interface modules. These signals are available for alternate usage providing

the bootloader and kernel are built to avoid conflicting interpretation of the lines. Please refer to Texas Instruments documentation (http://www.ti.com/product/omap4430) for a complete description of the available alternate signals. To modify this 'pin MUXing', edit the *duovero.h* file in the U-Boot bootloader source.

OMAP4 processors can boot from one of several sources and can, as such, always be recovered from a corrupted software state. Gumstix DuoVero COMs are set with peripheral boot priority, in order (1) USB and (2) MMC1 i.e. sysboot[5:0] = 0b000101. This boot order setting can be altered by the factory for volume orders.

2 Signals Internal to the Gumstix DuoVero COM

As shown in Figure 1 above, many processor interfaces are used directly on-board the DuoVero COM. Table 1 specifies which signals are used internally and as such their functionality should not be changed.

On-board MicroSD	
4-bit SD interface	SDMMC1
Card Detect	PMIC MMC Detect
Wi-Fi and Bluetooth Module	
4-bit SD interface	SDMMC5
Bluetooth PCM	McBSP1
I2C Control Interface	I2C4
Clock	CLK_32KG
Reset (active low)	GPMC_A19 (GPIO 43)
Power Supply Enable	PMIC REGEN2
USB Host	
USB ULPI interface	USBB1
PHY Reset (active low)	GPMC_WAIT1 (GPIO 62)
PHY Reference Clock	FREF_CLK3_OUT
PMIC	
Control Interface	I2C1
Interrupt Line	SYS_NINT1
MSECURE	FREF_CLK0_OUT (GPIO 6)
Audio Codec	
Control Interface	I2C1
Interrupt Line	SYS_NINT2
Audio Interface	PDM
Power On	USBB2_ULPITLL_NXT (GPIO 160)
LED Controls on Board	
D1: Red	Wi-Fi active
D2: Blue	Bluetooth active
D3: Green	Board active
Board Version Identity*	
BID[0:5]	USBB2_ULPITLL_DAT[0:5] (GPIO[161:166])

* GPIOs sampled at boot in order to perform version specific configuration.

Table 1: Internal Signals

2.1 SD Card Cage

A microSD card slot on the Gumstix DuoVero COM is connected to the processor's bootable SDMMC1 interface. An active high card detect line is connected to the MMC card detect ball on the PMIC.

2.2 Wireless Module

Bluetooth and Wi-Fi support is provided on some COM modules by Wi2Wi's W2CBW0015 chip (http://www.wi2wi.com/products/datasheets/W2CBW0015.pdf). The wireless IC module is powered by a seperate supply controlled by PMIC signal REGEN1; the GPMC_A19 line from the process is an active-low reset. The chip can be controlled via I2C bus 4 and the 32kHz gated-clock furnished by the OMAP4. 802.11b/g/n modes as well as micro-access point mode are supported directly in the linux kernel. The OMAP4 communicates with the modules via the SDMMC5 bus. The module provides support for Bluetooth 3.0 and the Bluetooth audio data is available through the McBSP1 interface. The blue LED indicated bluetooth activity and the Red LED indicates Wi-Fi activitiy.

2.3 USB

A USB host connection is broken out over the J2 connector. The USBB1 ULPI signals from the OMAP4 drive this interface through a USB3326 interface chip clocked by FREF_CLK3_OUT. A USB On-The-Go (OTG) interface available on J1 connector is controlled directly by the processor's USBA0 interface.

2.4 PMIC

Power management on the Gumstix DuoVero COM uses the TWL6030 PMIC. Several lines are available externally to support the design of expansion boards: PWRON, NRESWARM, SYSEN, REGEN1, VBACKUP, VDD_VAUX2, ADC lines and PWM lines. For more detail on the usage of these signals, refer to the documentation for the TWL6030 module. Internally, the PMIC is controlled by the processor through the I2C1 control interface as well the the dedicated SmartReflex I2C channel. Access to protected registers can be locked using the MSECURE line on processor GPIO 6. The processor receives interrupts on SYS_NINT1.

2.5 Audio Codec

The TWL6040 audio codec provides external differential audio interfaces: the HMIC audio input and the stereo HSL/HSR audio output†. The codec can be controlled via the I2C1 interface. Audio streams can be accessed through the PDM interface. The processor receives interrupts from the codec on the SYS_NINT2 line and can use GPIO 160 to enable the chip.

2.6 Interface Notes

The EMU0 and EMU1 balls are pull high on the Gumstix DuoVero COM to support JTAG operation. The HDQ line and all I2C interfaces with the exception of the dedicated Smart Reflex interface are pulled to 1.8V to ensure correct operation. The green LED D3 is controlled by GPIO173 and is conventionally used as a system heartbeat indicator.

3 Externally Available Signals

Signals are accessible via the J1 and J2 interface connectors on each Gumstix DuoVero COM. The following tables indicate the available signals grouped by their default function; these signals can be MUXed for a different purpose. The interfaces available through pin-muxing are, in general, not described below. The *duovero_mux_data.h* file in the U-boot bootloader source code implements this MUXing; it is both the definitive reference and the place to make changes as required. The "Internal Connection" column indicates where the signal originates on the DuoVero COM and, if required, where users should look for further details.

3.1 Serial Interfaces

Several UART, I2C, 1-wire, McBSP and SPI interfaces are available on the J1 and J2 external connectors and some pins can be muxed to provide additional interfaces. The Chateau expansion board (http://pubs.gumstix.com/boards/CHATEAU/PCB40022-R3872/PCB30002.pdf) provides a sample implementation of UART3 used as a USB console port.

External Connection	Signal	Internal Connection
J2 Pin 50	HDQ_SIO (GPIO 127)	OMAP AA27
J2 Pin 49	I2C3_SDA (GPIO 131)	OMAP Y27
J2 Pin 48	I2C3_SCL (GPIO 130)	OMAP W27
J1 Pin 70	I2C2_SDA (GPIO 129)	OMAP D26
J1 Pin 3	I2C2_SCL (GPIO 128)	OMAP C26
J2 Pin 17	UART2_RX (GPIO 125)	OMAP AA25
J2 Pin 18	UART2_TX (GPIO 126)	OMAP AA26
J2 Pin 20	UART3_CTS (GPIO 141)*	OMAP F27
J2 Pin 21	UART3_RTS (GPIO 142)*	OMAP F28
J2 Pin 23	UART3_RX (GPIO 143)*	OMAP G27
J2 Pin 22	UART3_TX (GPIO 144)*	OMAP G28
J2 Pin 7	UART4_RX (GPIO 155)	OMAP AG20
J2 Pin 6	UART4_TX (GPIO 156)	OMAP AH19
J2 Pin 8	MCSPI1_CS3 (GPIO 140)	OMAP AH23
J2 Pin 9	MCSPI1_CS2 (GPIO 139)	OMAP AG23
J2 Pin 10	MCSPI1_CS1 (GPIO 138)	OMAP AF23
J2 Pin 13	MCSPI1_CS0 (GPIO 137)	OMAP AE23
J2 Pin 11	MCSPI1_CLK (GPIO 134)	OMAP AF22†
J2 Pin 12	MCSPI1_SIMO (GPIO 136)	OMAP AG22
J2 Pin 14	MCSPI1_SOMI (GPIO 135)	OMAP AE22
J2 Pin 19	MCSPI4_CS0 (GPIO 154)	OMAP AE20
J2 Pin 24	MCSPI4_SIMO (GPIO 152)	OMAP AF20
J2 Pin 25	MCSPI4_SOMI (GPIO 153)	OMAP AF21
J2 Pin 26	MCSPI4_CLK (GPIO 151)	OMAP AE21
J2 Pin 55	ABE_BSP2_DR (GPIO 111)	OMAP AD26
J2 Pin 54	ABE_BSP2_CLKX (GPIO 110)	OMAP AD27
J2 Pin 53	ABE_BSP2_DX (GPIO 112)	OMAP AD25
J2 Pin 52	ABE_BSP2_FSX (GPIO 113)	OMAP AC28
J2 Pin 51	ABE_CLKS (GPIO 118)	OMAP AH26

* console port
† includes anti-reflection resistor

Table 2: Serial Port Signals

3.2 Camera Signals

Two MIPI-compliant LVDS camera interfaces, the 5-lane CSI21 interface and the 2-lane CSI22 interface, as well as a several camera control lines are broken out on the J2 connector on the Gumstix DuoVero COM. Note: the CSI21_D* and CSI22_D* signals are marked as input-only if muxed into GPIO mode.

External Connection	Signal	Internal Connection
J2 Pin 31	CSI21_DX0 (GPIO 67)	OMAP R26
J2 Pin 30	CSI21_DY0 (GPIO 68)	OMAP R25
J2 Pin 37	CSI21_DX1 (GPIO 69)	OMAP T26
J2 Pin 36	CSI21_DY1 (GPIO 70)	OMAP T25
J2 Pin 39	CSI21_DX2 (GPIO 71)	OMAP U26
J2 Pin 38	CSI21_DY2 (GPIO 72)	OMAP U25
J2 Pin 40	CSI21_DX3 (GPIO 73)	OMAP V26
J2 Pin 41	CSI21_DY3 (GPIO 74)	OMAP K25
J2 Pin 42	CSI21_DX4 (GPIO 75)	OMAP W26
J2 Pin 43	CSI21_DY4 (GPIO 76)	OMAP W25
J2 Pin 34	CSI22_DX0 (GPIO 77)	OMAP M26
J2 Pin 35	CSI22_DY0 (GPIO 78)	OMAP M25
J2 Pin 33	CSI22_DX1 (GPIO 79)	OMAP N26
J2 Pin 32	CSI22_DY1 (GPIO 80)	OMAP N25
J2 Pin 44	FREF_CLK1_OUT (GPIO 181)	OMAP AA28
J2 Pin 45	CAM_SHUTTER (GPIO 81)	OMAP T27
J2 Pin 46	CAM_STROBE (GPIO 82)	OMAP U27
J2 Pin 47	CAM_RESET (GPIO 83)	OMAP V27

Table 3: Camera Signals

3.3 Display Signals

A 5-lane MIPI compliant display interface, DSI1, is broken out on the J2 connector and the standard lines to drive an HDMI interface including DDC are available on the J1 connector. An example use of the HDMI signals can be seen on the Parlor board (http://pubs.gumstix.com/boards/PARLOR/PCB40002-R3902/PCB40002.pdf).

External Connection	Signal	Internal Connection
J1 Pin 30	HDMI_CLOCKX	OMAP C11
J1 Pin 29	HDMI_CLOCKY	OMAP D11
J1 Pin 28	HDMI_D0X	OMAP D10
J1 Pin 27	HDMI_D0Y	OMAP C10
J1 Pin 25	HDMI_D1X	OMAP C9
J1 Pin 26	HDMI_D1Y	OMAP D9
J1 Pin 24	HDMI_D2X	OMAP C8
J1 Pin 23	HDMI_D2Y	OMAP D8
J1 Pin 36	HDMI_DDC_SCL (GPIO 65)	OMAP A8
J1 Pin 37	HDMI_DDC_SDA (GPIO 66)	OMAP B8
J1 Pin 38	HDMI_HPD (GPIO 63)	OMAP B9
J1 Pin 39	HDMI_CEC (GPIO 64)	OMAP B10
J1 Pin 40	HDMI_LS_OE* (GPIO 41)	OMAP A18
J2 Pin 66	DSI1_DX0	OMAP P3
J2 Pin 65	DSI1_DY0	OMAP P4
J2 Pin 67	DSI1_DX1	OMAP N3
J2 Pin 68	DSI1_DY1	OMAP N4
J2 Pin 3	DSI1_DX2	OMAP M3
J2 Pin 4	DSI1_DY2	OMAP M4
J2 Pin 1	DSI1_DX3	OMAP L3
J2 Pin 2	DSI1_DY3	OMAP L4
J2 Pin 69	DSI1_DX4	OMAP K3
J2 Pin 70	DSI1_DY4	OMAP K4

* This GPIO allocation is merely by convention.

Table 4: Display Signals

3.4 Analog Signals

The Parlor expansion board (http://pubs.gumstix.com/boards/PARLOR/PCB40002-R3902/B40002.pdf) provide a sample implementation of audio and breaks out several other analog lines.

External Connection	Signal	Internal Connection
J1 Pin 45	GPADC_IN6	TWL6030
J1 Pin 46	GPADC_IN2	TWL6030
J1 Pin 47	GPADC_IN5	TWL6030
J1 Pin 48	GPADC_IN3	TWL6030
J1 Pin 49	GPADC_IN4	TWL6030
J1 Pin 50	GPADC_VREF4	TWL6030
J1 Pin 51	GPADC_START	TWL6030
J1 Pin 43	PMIC_PWM1	TWL6030
J1 Pin 44	PMIC_PWM2*	TWL6030
J2 Pin 62	HFL_P	TWL6040
J2 Pin 61	HFL_N	TWL6040
J2 Pin 60	HFR_P	TWL6040
J2 Pin 59	HFR_N	TWL6040
J2 Pin 64	AUDIN_P	TWL6040
J2 Pin 63	AUDIN_N	TWL6040

Table 5: Analog Signals on the Gumstix DuoVero COM

* Additional PWM and quadrature capture signals can be muxed from the processor.

3.5 Control Signals

All expansion boards need to provide power and need to interface with some of these control signals.

External Connection	Signal	Internal Connection
J1 Pin 58	PWRON	TWL6030
J1 Pin 57	PMIC_NRESWARM	TWL6030
J1 Pin 61	SYSEN	TWL6030
J1 Pin 62	REGEN1	TWL6030
J2 Pin 58	VDD_VAUX2	TWL6030
J1 Pin 55	VBACKUP	TWL6030
J1 Pin 41	VSYSTEM	Power
J1 Pin 42	VSYSTEM	Power
J1 Pin 22	GND	Power
J1 Pin 31	GND	Power
J2 Pin 5	GND	Power

Table 6: Control Signals on the Gumstix DuoVero COM

3.6 High Speed Buses: MMC, USB Host and OTG

High-bandwidth communication is possible over several standard interfaces as shown, for example, on the Parlor (http://pubs.gumstix.com/boards/PARLOR/PCB40002-R3902/B40002.pdf) expansion board.

External Connection	Signal	Internal Connection
J2 Pin 16	SDMMC3_CLK*	OMAP AE9
J2 Pin 15	SDMMC3_CMD*	OMAP AG10
J2 Pin 17	SDMMC3_DAT0 (UART2_RX pin)*	OMAP AA25
J2 Pin 18	SDMMC3_DAT1 (UART2_TX pin)*	OMAP AA26
J2 Pin 29	USBH_DM	USB3326
J2 Pin 28	USBH_DP	USB3326
J2 Pin 27	USBH_VBUS	USB3326
J1 Pin 34	USBOTG_DM	OMAP B4
J1 Pin 33	USBOTG_DP	OMAP B5
J1 Pin 32	USBOTG_ID	TWL6030
J1 Pin 35	USBOTG_VBUS_IN	TWL6030

Table 7: High Speed Buses on the Gumstix DuoVero COM

* not mux mode 0

3.7 Conventional Allocations

Several signals are broken out simply as GPIOs. Typically, these particular signals are chosen because they provide access through muxing to otherwise inaccessible signals. On the Gumstix expansion boards, these GPIOs may be used, by convention, for a specific purpose. There is no requirement that other expansion boards conform to these choices; this merely communicates the intended usage and describes how open-source software should be configured for this board.

External Connection	Signal	CPU Ball
J2 Pin 57	GPIO121 – user push button	OMAP AG24
J2 Pin 56	GPIO122 – user LED	OMAP AH24
J1 Pin 52	GPIO44 – ethernet interrupt	OMAP B19
J1 Pin 53	GPIO45 – ethernet reset	OMAP B20
J1 Pin 54	GPIO48 – ethernet mdix	OMAP C20
J1 Pin 56	GPIO46 – ethernet pme	OMAP A21

Table 8: Conventional GPIO Usage

3.8 Memory Bus Signals

The General-Purpose Memory Controller (GPMC) provides a direct, memory-mapped interface to the processor. This is useful for interfacing FPGAs, attaching external memories, or, as shown on the Parlor (http://pubs.gumstix.com/boards/PARLOR/PCB40002-R3902/B40002.pdf) board, providing a network interface.

External Connection	Signal	Internal Connection
J1 Pin 19	GPMC_AD0	OMAP C12
J1 Pin 18	GPMC_AD2	OMAP C13
J1 Pin 17	GPMC_AD3	OMAP D13
J1 Pin 16	GPMC_AD1	OMAP D12
J1 Pin 15	GPMC_AD4	OMAP C15
J1 Pin 14	GPMC_AD5	OMAP D15
J1 Pin 13	GPMC_AD6	OMAP A16
J1 Pin 12	GPMC_AD7	OMAP B16
J1 Pin 11	GPMC_AD9 (GPIO 33)	OMAP D16
J1 Pin 10	GPMC_AD8 (GPIO 32)	OMAP C16
J1 Pin 9	GPMC_AD11 (GPIO 35)	OMAP D17
J1 Pin 8	GPMC_AD10 (GPIO 34)	OMAP C17
J1 Pin 7	GPMC_AD12 (GPIO 36)	OMAP C18
J1 Pin 6	GPMC_AD13 (GPIO 37)	OMAP D18
J1 Pin 5	GPMC_AD15 (GPIO 39)	OMAP D19
J1 Pin 4	GPMC_AD14 (GPIO 38)	OMAP C19
J1 Pin 59	GPMC_CLK (GPIO 55)	OMAP B22
J1 Pin 67	GPMC_NADV_ALE (GPIO 56)	OMAP D25
J1 Pin 60	GPMC_NBE0 (GPIO 59)	OMAP C23
J1 Pin 64	GPMC_NBE1 (GPIO 60)	OMAP D22
J1 Pin 63	GPMC_NCS3 (GPIO 53)	OMAP C22
J1 Pin 66	GPMC_NCS4 (GPIO 101)	OMAP A24
J1 Pin 1	GPMC_NCS5* (GPIO 102)	OMAP B24
J1 Pin 65	GPMC_NCS6 (GPIO 103)	OMAP C24
J1 Pin 21	GPMC_NOE	OMAP B11
J1 Pin 20	GPMC_NWE	OMAP B12
J1 Pin 2	GPMC_NWP (GPIO 54)	OMAP C25
J1 Pin 69	GPMC_WAIT0 (GPIO 61)	OMAP B26
J1 Pin 68	GPMC_WAIT2 (GPIO 100)	OMAP D23

Table 9: External Memory Bus Signals of the Gumstix DuoVero COM

* conventional chip select for first Ethernet controller

4 Expansion Board Design Recommendations

To help improve the design of a custom expansion board for the Gumstix DuoVero series, this list offers hints and tips with some potential design pitfalls to be avoided:

1. Use the SYSEN line to protect any IO pins to the OMAP CPU. SYSEN is brought high when the DuoVero is ready to communicate; driving GPIOs before this point can damage the processor.
2. For high-speed signal lines, consider adding small-valued series resistors to limit signal reflections. Users have reported success adding 33 ohm series resistors to the CLK and CMD lines of the MMC3 external interface.
3. The white DuoVero retaining spacers (https://www.gumstix.com/store/product_info.php?products_id=238) should be used for a PCB of thickness 48mils (1.22mm) with standard manufacturing tolerances.
4. The blue DuoVero retaining spacers (https://www.gumstix.com/store/product_info.php?products_id=278) should be used for a PCB of thickness 62mils (1.57mm) with standard manufacturing tolerances.
5. Mounting hole diameter should be 1.65mm.

Other key links for designing with Gumstix can be found here: https://www.gumstix.com/cbg-industrial-strength.html

5 FAB Revision of the Gumstix DuoVero COM

From time to time, minor changes are made to the design of the PCB in order to make new features available, adjust for component supply or make minor improvements to the design. To the greatest extent possible, changes are invisible to the user and are backward compatible with previous revision of the COM. Gumstix does not anticipate making any major developments or design changes to the DuoVero COM series.

Changes made since DuoVero COMs FAB Revision R3800:

FAB Revision R3800 First Production Release

The term *FAB* refers specifically to the printed circuit board (PCB) not the components populated on that PCB. The FAB revision number is silk-screened directly on the PCB. The revision number of the assembled board is printed on the white label of each COM. The identifying information for DuoVero COMs is discussed in more detail at http://pubs.gumstix.com/boards/AA_README.txt.

DuoVero COMs are interchangeable with individual models providing different features.

6 Physical Design

Each Gumstix DuoVero COM mates with a Gumstix or custom expansion board via the pair of 70-pin connectors located on the bottom side of the COM. These connectors, identified as J1 and J2, mate with Hirose DF40C series connectors such as DF40C-70DS-0.4V (http://www.hirose.co.jp/cataloge_hp/e68440018.pdf).

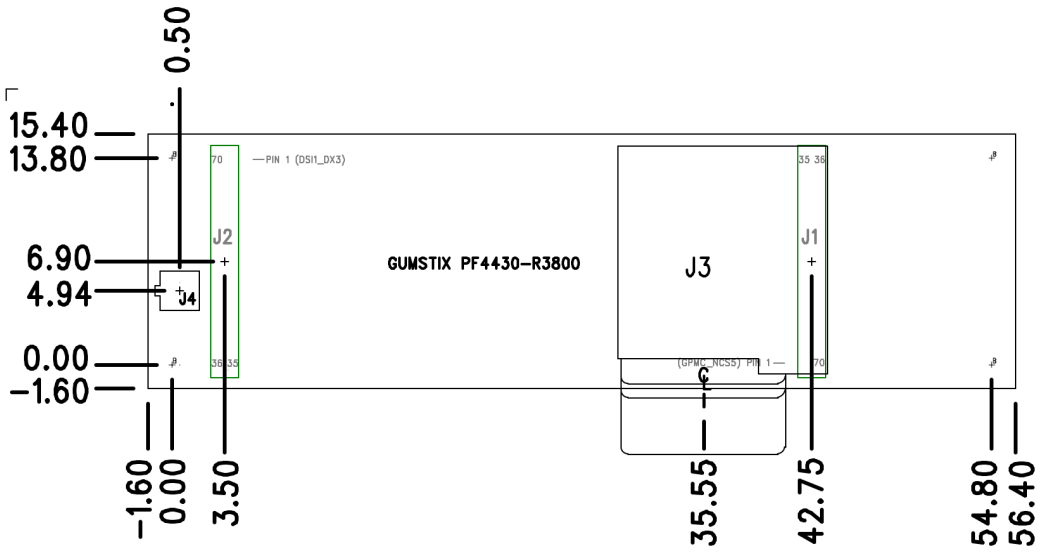

Figure 2: DuoVero COM Physical Design

The board to board spacing for DuoVero COMs is 1.5mm but taller connectors are available. When designing custom expansion boards for DuoVero COMs, be cautious placing components directly beneath the DuoVero COM, to avoid mechanical interference problems.

7 Additional Resources

This System Reference Manual is unique to the design and use of the Gumstix DuoVero COMs. Resources from Gumstix and related suppliers that may also be of interest include:

Getting Started http://gumstix.org/get-started.html

Software Development http://gumstix.org/software-development.html

OMAP4430 Applications Processor http://www.ti.com/product/omap4430

eLinux OMAP4430 HQ http://elinux.org/OMAP4430

TWL6030 PMIC http://www.ti.com/product/twl6030

TWL6040 Audio Codec http://www.ti.com/product/twl6040

USB3320 Interface Chip http://www.smsc.com/index.php?tid=143&pid=211

W2WCB0015 Wireless Module http://wi2wi.com/wireless.php

8 Document History

- Document Revision 0.1

  Derived from Overo System Reference Manual.

- Document Revision 0.2

  Correct J2 Pin 31 breakout typo (with thanks to Will Bryan).

- Document Revision 0.3

  Correct UART3_{CTS|RTS} & HDMI_D0Y breakout typo (with thanks to Philip Evans).