Gumstix™ Pepper Single Board Computer

System Reference Manual—Version 0.1
Last Revised: June 16, 2013

Gumstix, Inc. shall have no liability of any kind, express or implied, arising out of the use of the Information in this document, including direct, indirect, special or consequential damages.

Gumstix, Inc. may have patents, patent applications, trademarks, copyrights, trade secrets or other intellectual property rights pertaining to Gumstix products described in this document (collectively “Gumstix Intellectual Property").

Except as expressly provided in any written license or agreement from Gumstix, Inc., this document and the information contained therein does not create any license to Gumstix’s Intellectual Property.

The Information contained herein is subject to change without notice. Revisions may be issued regarding changes and/or additions.

This System Reference Manual is a general reference for the Gumstix Pepper single board computer (SBC). It describes the components, the internal system connections, and the external interfaces for users writing software or designing systems that include the Gumstix Pepper SBC.

Physical models of the Gumstix Pepper SBC are published at http://pubs.gumstix.com/boards/COMS/.

Software information can be found online (http://www.gumstix.org/software-development.html).

Contents

List of Tables

List of Figures

1 Product Overview

Figure 1 shows the main components of the Gumstix Pepper SBC which includes a Texas Instruments OMAP™ AM3359 applications processor (ARM® Cortex™-A8 core), 512MB of DDR2 RAM, a TPS62517B power management module, the TLV320AIC3106 audio codec, gigabit Ethernet, a 4.3" touchscreen, an accelerometer and a W2CBW0015 Wi-Fi™ & Bluetooth™ module.

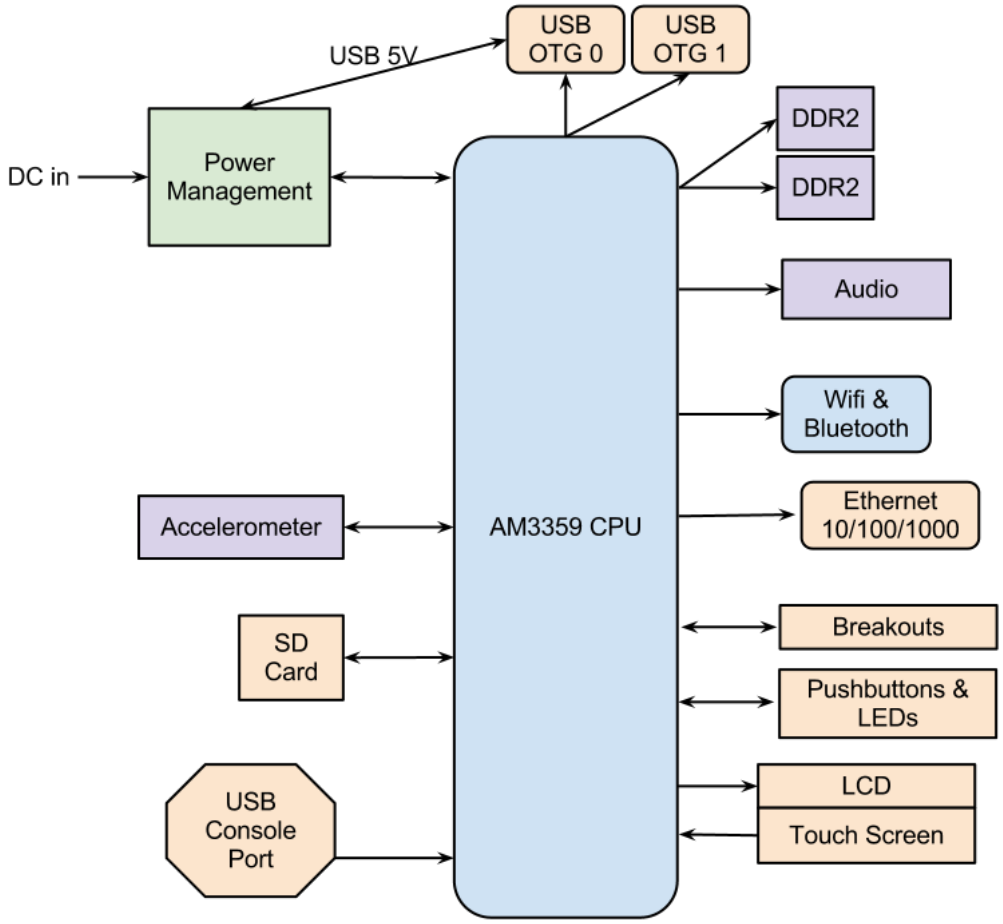

Figure 1: Gumstix Pepper SBC System Architecture

1.1 System Configuration

The Gumstix Pepper SBC is designed to be a cost-effective yet powerful platform useful in a range of embedded applications. In addition to the features on board, there is an expansion header which breaks out SPI (2 chip selects), dual I2C buses, a UART with hardware flow control, an SDIO interface, GPIOs, and power rails.

The AM3359 processor can boot from one of several sources and can, as such, always be recovered from a corrupted software state. Gumstix Pepper SBCs are configured with boot order MMC0, SPI0, UART0, USB0 with a 24MHz clock, RGMII (no-delay) support, and CLKOUT1 enabled i.e. sysboot = 0b01000000 0b11110111. This boot order setting can be altered by the factory for volume orders.

CE and FCC approvals for the Wi2Wi Bluetooth™ and Wi-Fi™ module can be found online (http://pubs.gumstix.com/documents/Approvals/Wi2Wi/W2CBW0015).

2 Electrical Design

This section details the significant components of the system shown in Figure 1 above describing the bus-level interconnections and the power system design.

Table 1 offers a concise description of the signals used on-board. As such their functionality should not be changed. Note all ball references on the processor are for the ZCZ package.

Table 1: Internal Signals

On-board MicroSD	
4-bit SD interface	MMC0
Card Detect	MMC0 Detect (ball C15)
Wi-Fi and Bluetooth Module	
4-bit SDIO interface	SDIO2
Bluetooth PCM	Audio Codec Secondary PCM
I2C Control Interface	I2C0
Reset (active low)	GPIO 56 (ball V16)
Power Down (active low)	GPIO 30 (ball T17)
PMIC	
Control Interface	I2C0
Audio Codec	
Control Interface	I2C0
Audio Interface	McASP0
Reset (active low)	GPIO 48 (ball R13)
eMMC (non-populated)	
Control Interface	MMC1
Reset (active low)	GPIO 64 (ball U17)
Board ID EEPROM	
Control Interface	I2C0
LCD Touchscreen	
Display Interface	24-bit LCD Data
Display Enable	GPIO 59 (ball V17)
Analog Touch Interface	AIN[0:3]
USB	
USB Console	UART0
USB OTG 0 (J4 connector)	USB0
USB OTG 0 Overcurrent (active low)	GPIO 57 (ball U16)
USB OTG 1 (J5 connector)	USB1
USB OTG 1 Overcurrent (active low)	GPIO 58 (ball T16)
Accelerometer	
Control Interface	I2C0
Interrupt	GPIO 68 (ball U6)

Ethernet	
Management Interface	MDC and MDIO
Data Interface	RGMII1
Interrupt (active low)	GPIO 91 (ball H18)
PHY Reset (active low)	GPIO 96 (ball H16)
LEDs on Board	
D1 (Red) System active	PMIC VLDO2
D2 (Green) USB Console active	
D3 (Blue) User LED 1	GPIO 52 (ball R14)
D4 (Red) User LED 2	GPIO 53 (ball V15)
D6 (Green) Wi-Fi active	
D8 (Blue) Bluetooth active	
Buttons on Board	
S1 Reset	PMIC PB_IN
S2 User LED 1	GPIO 54 (ball U15)
S3 User LED 2	GPIO 55 (ball T15)

A more detailed description of the electrical behaviour of each interface or function is given in the following sections

2.1 SD Card Slot

The microSD card slot on the Gumstix Pepper SBC is connected to the processor's bootable MMC0 interface. An active high card detect line is connected to the MMC0_SDCD line (MUX Mode 5 for ball C15). The card is powered by PMIC LDO3.

2.2 Wireless Module

Bluetooth and Wi-Fi support is provided by Wi2Wi's W2CBW0015 chip (http://www.wi2wi.com/products/datasheets/W2CBW0015.pdf). The wireless IC module is powered by a separate, uncontrolled, 3.3V supply and clocked by the system 32kHz clock. The chip can be powered down using active low GPIO 30 and reset by active low GPIO56. The chip can be controlled via I2C bus 0. 802.11b/g/n modes as well as micro-access point mode are supported directly in the Linux kernel. The OMAP3 communicates with the modules via the SDIO2 (muxed) bus. The module provides support for Bluetooth 3.0 and the Bluetooth audio data is available through the secondary PCM interface of the audio codec. The blue LED indicated bluetooth activity and the green LED indicates Wi-Fi activity.

2.3 USB

Two USB On-The-Go (OTG) interfacee, USB0 and USB1, are accessible on the J4 and J5 micro-AB USB connectors. In host mode, a 5V boost regulator drives the VBUS line on each connector; each can be separately enabled using the respective DRVVBUS signal. Over-current situations for USB0 and USB1 are indicated to the processor (active low) on GPIO 57 (ball U16) and GPIO 58 (ball T16) respectively.

2.4 PMIC

Power management on the Gumstix Pepper SBC uses the TPS62517B PMIC. Several lines are available externally to support the design of expansion boards: PWRON, NRESWARM, SYSEN, REGEN1, VBACKUP, and VDD_VAUX2 lines. For more detail on the usage of these signals, refer to the documentation for the TPS62517B. Internally, the PMIC is controlled by the processor through the I2C0 control interface. Switch S1 grounds the PB_IN signal on the PMIC; a long press will reset the system. The analog multiplexer (mux) output is connected to the processor's analog input AIN7. The system voltage can be monitored on the analog mux input through a resistive divider.

2.5 Display

The J7 connector supports a 24-bit colour LCD screen as well as resistive touchscreen. J7 Pin 31 is an active high display enable signal driven by GPIO 57 (ball V17).

2.6 Ethernet

The processor drives the KSZ9021RN Gigabit Ethernet PHY on the RGMII1 interface and can control the PHY via the standard MDIO interface. The PHY is configured to advertise all capabilities on address 0 with no delay enabled. The device is powered by an uncontrolled regulator but can be reset using the active low GPIO 96 (ball H16). The interrupt drives GPIO 29 (H18).

2.7 Audio Codec

The TLV320AIC3106 audio codec processes PCM digital audio streams from the MCASP0 interface from the processor and the bluetooth PCM interface. It operates in I2C mode at address 0x1Bi and is clocked using an independent 12MHz oscillator. It is powered by LDO3 from the PMIC and can be controlled by the active low reset on GPIO 48 (ball R13). J9 provides a headset connection to the line/mic1 input and stereo HPL/HPR signals. Three additional differential audio outputs are accessible via test points described in Table 2.

Signal	Test Point
LEFT_LOP	TP3
LEFT_LOM	TP4
RIGHT_LOP	TP37
RIGHT_LOM	TP38
MONO_LOP	TP39
MONO_LOM	TP40

Table 2: Audio Test Points

2.8 Accelerometer

The LIS33DE accelerometer is available on I2C0 at address 0x1C. It is powered by PMIC LDO3 and can signal an interrupt on GPIO 68 (ball U6).

2.9 User IO

The Gumstix Pepper SBC includes two indicator LEDs and two pushbutton inputs as a convenience for users. A blue LED is controlled by GPIO 52 (ball R14) and a red LED is controlled by GPIO 53 (ball V15). User switch S2 connects GPIO 54 (ball U15)

to ground and user switch S3 connects GPIO 55 (ball T5) to ground.

2.10 eMMC

This component is not populated.

2.11 RAM

System memory is provided by dual 256MB (Micron MT47H256M8EB) DDR2 chips.

2.12 EEPROM

The board identity is stored on an AT24C01B-TH_B EEPROM accessible at address 0x51 on I2C0.

2.13 Interface Notes

System clock is 24MHz with a 32kHz real-time clock for low-power operation. The system console is connected to UART0 interface via a bus-powered FT230XQ chip. The I2C0 interface is pulled to 3.3V to ensure correct operation.

3 Software Configuration

This section discussed details of the system architecture that require software configuration. This includes the default pin multiplexing setup, conventional GPIO allocations and externally available signals.

3.1 I2C Addresses

Several on-board peripherals communicate on I2C Bus 0.

Audio Codec	0x1B
PMIC	0x24
EEPROM	0x50
Accelerometer	0x1D

Table 3: I2C Addresses

3.2 Pin Multiplexing

To support the peripherals on and off board, some balls on the processor are multiplexed to signals available in a mux mode other than zero.

Ball	Ball Name	Signal Name	Mux Mode
C18	ECAP0_IN_PWM0_OUT	GPIO0_7 (7)	7

Ball	Ball Name	Signal Name	Mux Mode
A15	XDMA_EVENT_INTR0	CLKOUT1 (24MHz)	3
D14	XDMA_EVENT_INTR1	CLKOUT2 (32kHz)	3
R13	GPMC_A0	GPIO1_16 (48)	7
V14	GPMC_A1	MMC2_DAT0	3
U14	GPMC_A2	MMC2_DAT1	3
T14	GPMC_A3	MMC2_DAT2	3
R14	GPMC_A4	GPIO1_20 (52)	7
V15	GPMC_A5	GPIO1_21 (53)	7
U15	GPMC_A6	GPIO1_22 (54)	7
T15	GPMC_A7	GPIO1_23 (55)	7
V16	GPMC_A8	GPIO1_24 (56)	7
U16	GPMC_A9	GPIO1_25 (57)	7
T16	GPMC_A10	GPIO1_26 (58)	7
V17	GPMC_A11	GPIO1_27 (59)	7
U7	GPMC_AD0	MMC1_DAT0	1
V7	GPMC_AD1	MMC1_DAT1	1
R8	GPMC_AD2	MMC1_DAT2	1
T8	GPMC_AD3	MMC1_DAT3	1
U8	GPMC_AD4	MMC1_DAT4	1
V8	GPMC_AD5	MMC1_DAT5	1
R9	GPMC_AD6	MMC1_DAT6	1
T9	GPMC_AD7	MMC1_DAT7	1
U10	GPMC_AD8	LCD_DATA23	1
T10	GPMC_AD9	LCD_DATA22	1
T11	GPMC_AD10	LCD_DATA21	1
U12	GPMC_AD11	LCD_DATA20	1
T12	GPMC_AD12	LCD_DATA19	1
R12	GPMC_AD13	LCD_DATA18	1
V13	GPMC_AD14	LCD_DATA17	1
U13	GPMC_AD15	LCD_DATA16	1
U18	GPMC_BEN1	MMC2_DAT3	3
V12	GPMC_CLK	MMC2_CLK	3
U9	GPMC_CSN1	MMC1_CLK	2
V9	GPMC_CSN2	MMC1_CMD	2
T13	GPMC_CSN3	MMC2_CMD	3
T17	GPMC_WAIT0	GPIO0_30 (12)	7
U6	GPMC_WEN	GPIO2_4 (68)	7
U17	GPMC_WPN	GPIO0_31 (31)	7
J17	MII1_RX_DV	RGMII1_RCTL	2
J16	MII1_TX_EN	RGMII1_TCTL	2
J15	MII1_RX_ER	I2C1_SCL	3
L18	MII1_RX_CLK	RGMII1_RCLK	2
K18	MII1_TX_CLK	RGMII1_TCLK	2
H16	MII1_COL	GPIO3_0 (96)	7
H17	MII1_CRS	I2C1_SDA	3
M16	MII1_RXD0	RGMII1_RD0	2
L15	MII1_RXD1	RGMII1_RD1	2
L16	MII1_RXD2	RGMII1_RD2	2
L17	MII1_RXD3	RGMII1_RD3	2
K17	MII1_TXD0	RGMII1_TD0	2
K16	MII1_TXD1	RGMII1_TD1	2
K15	MII1_TXD2	RGMII1_TD2	2

Ball	Ball Name	Signal Name	Mux Mode
J18	MII1_TXD3	RGMII1_TD3	2
H18	RMII1_REF_CLK	GPIO0_29 (29)	7
C15	SPI_CS1	MMC0_SDCD	5

Table 4: Pin Multiplexing

4 Externally Available Signals

Signals are accessible via the 2x20 pin J6 header and, unless otherwise noted, use 3.3V logic. Figure 2 indicates the available signals grouped by their default function; these signals can be multiplexed for a different purpose. The interfaces available through pin-muxing are, in general, not described below; please refer to Texas Instruments documentation (http://www.ti.com/product/am3359) for a complete description of the available alternate signals. To modify this 'pin MUXing', edit the *mux.c* file in the U-Boot bootloader source. Pin 1 is denoted by a square pad; pin 2 is beside pin 1 towards the center of the board.

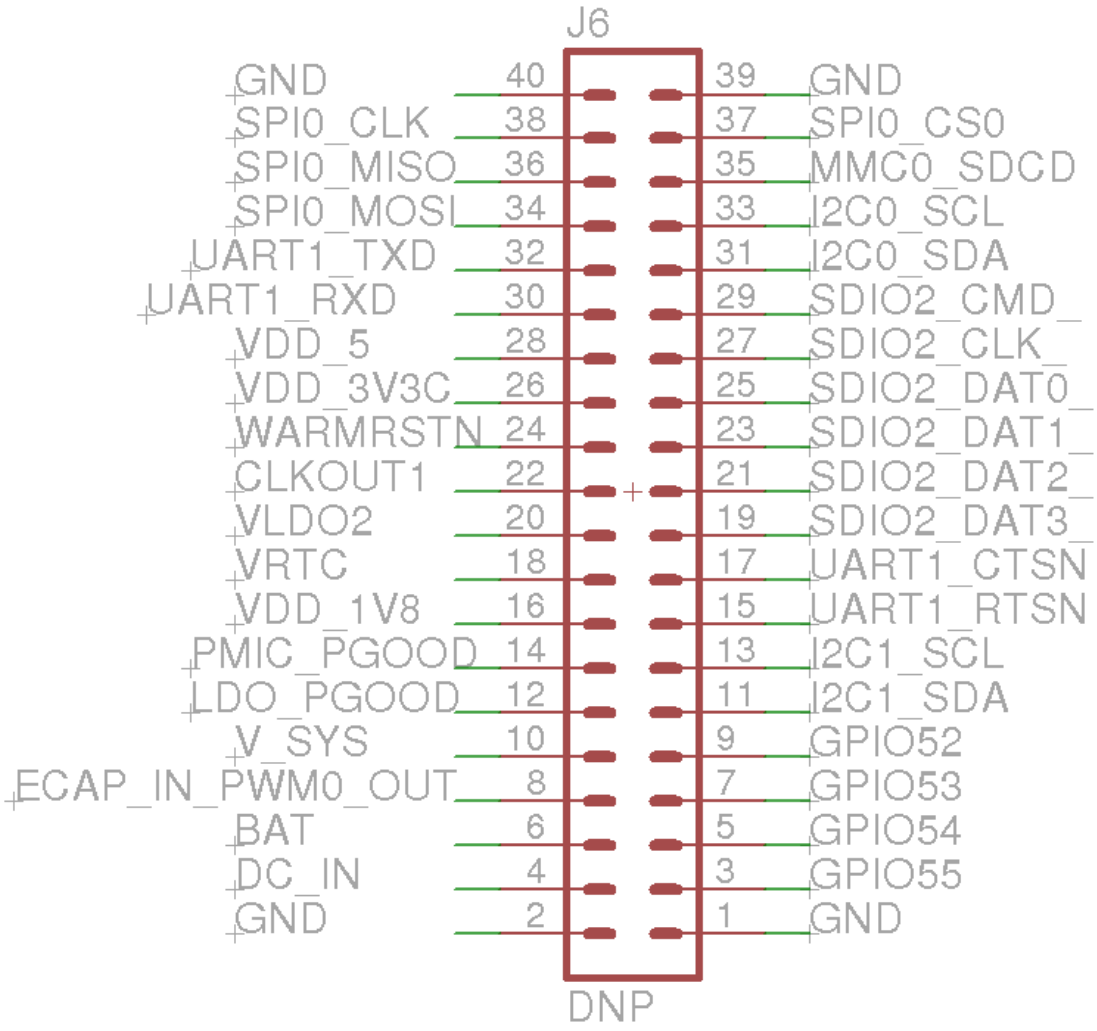

Figure 2: J6 External Header

5 Additional Resources

This System Reference Manual is unique to the design and use of the Gumstix Pepper single board computer. Resources from Gumstix and related suppliers that may also be of interest include:

Getting Started http://gumstix.org/get-started.html

Software Development http://gumstix.org/software-development.html

AM3359 Applications Processor http://www.ti.com/product/am3359

TPS65217B PMIC http://www.ti.com/product/tps65217b

TLV320AIC3106 Audio Codec http://www.ti.com/product/tlv320aic3106

W2WCB0015 Wireless Module http://wi2wi.com/wireless.php

Comments, questions, suggestions? Send a message to the Gumstix Users mailing list at gumstix-users@lists.sourceforge.net.

6 Document History

- Document Revision 0.1

  Derived from Overo System Reference Manual.

